



Digital Transistors (Built-in Resistors)

Features

- Epoxy meets UL-94 V-0 flammability rating
- Moisture Sensitivity Level 1
- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors
- Surface mount package ideally Suited for Automatic Insertion
- NPN

Mechanical Data

Package: SOT-323

Terminals: Tin plated leads, solderable per J-STD-002 and JESD22-B102

Marking: TL



DTC144WUA

Electrical Characteristics (Ta=25 unless otherwise specified)

ITEM	SYMBOL	UNIT	CONDITIONS	MIN	TYP	MAX
Input voltage	$V_{I(off)}$	V	$V_{CC}=5V, I_c=100\mu A$	0.8		
	$V_{I(on)}$	V	$V_o=0.3V, I_c=2mA$			4
Output voltage	$V_{O(on)}$	V	$I_o / I_i = 10mA/0.5 mA$			0.3
Input current	I_i	mA	$V_i=5V$			160
Output current	$I_{O(off)}$	μA	$V_{CC}=50V, V_i=0$			0.5
DC current gain	G_I		$V_o=5V, I_o = 5mA$	56		
Input resistance	R_1			33	47	61
Resistance ratio	R_2/R_1			0.37	0.47	0.57
Transition frequency	f_T	MHz	$V_o=10V, I_o=5mA, f=100MHz$		250	

Thermal Characteristics

Parameter	Symbol	Unit	Value
Thermal resistance, junction-to-ambient	$R_{-A}^{(1)}$	$^{\circ}W$	625
Thermal resistance, junction-to-case	$R_{-C}^{(1)}$	$^{\circ}W$	500

Note:

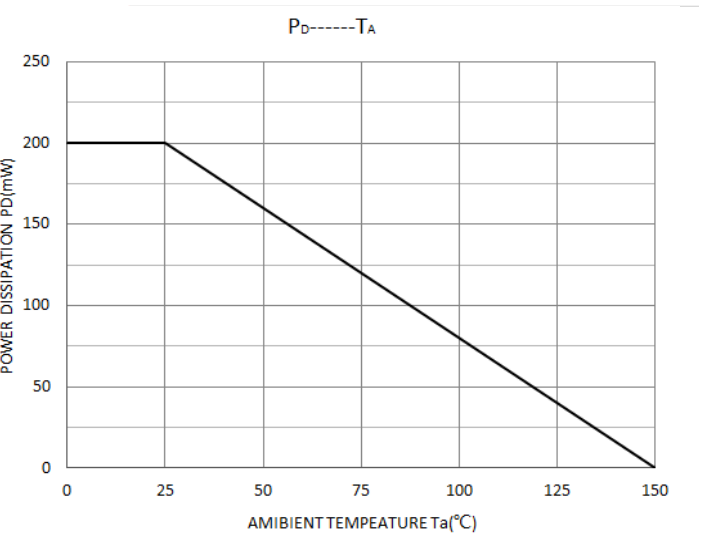
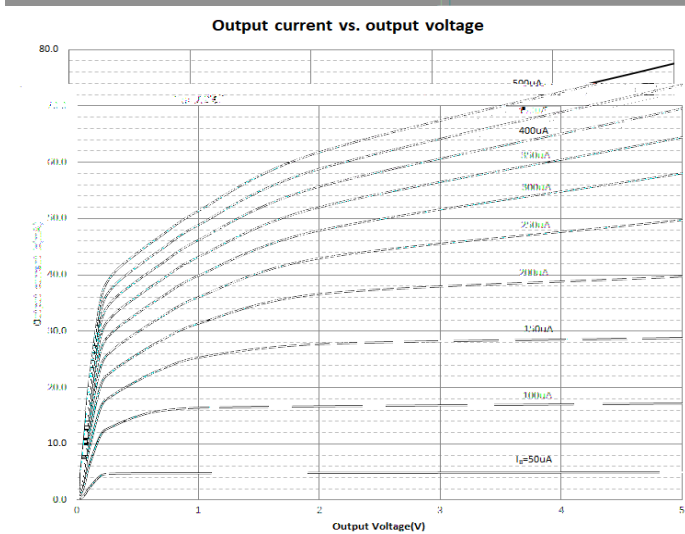
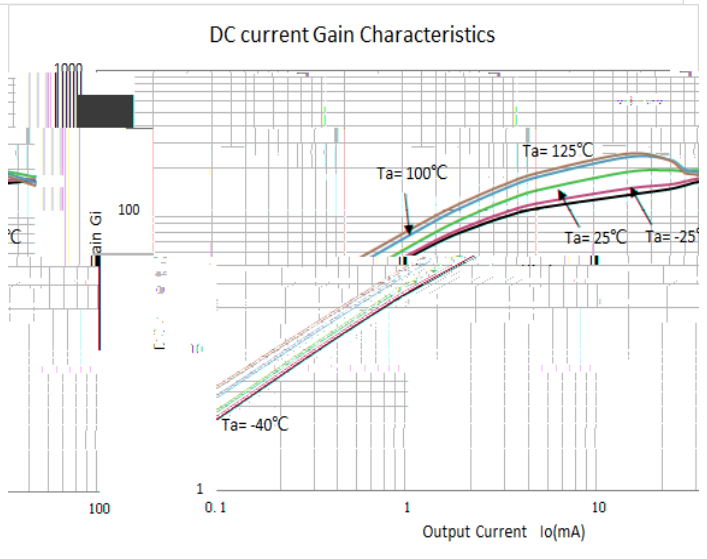
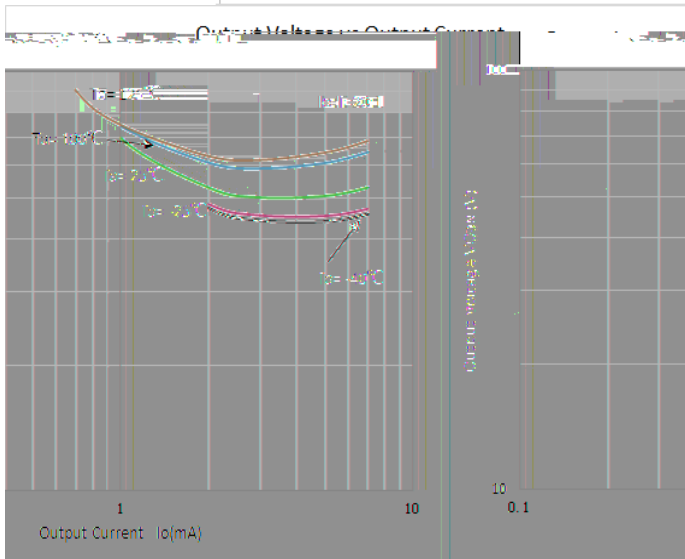
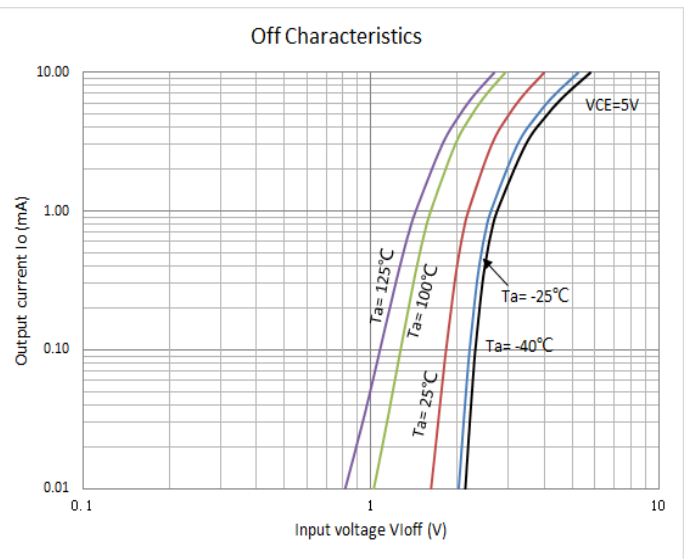
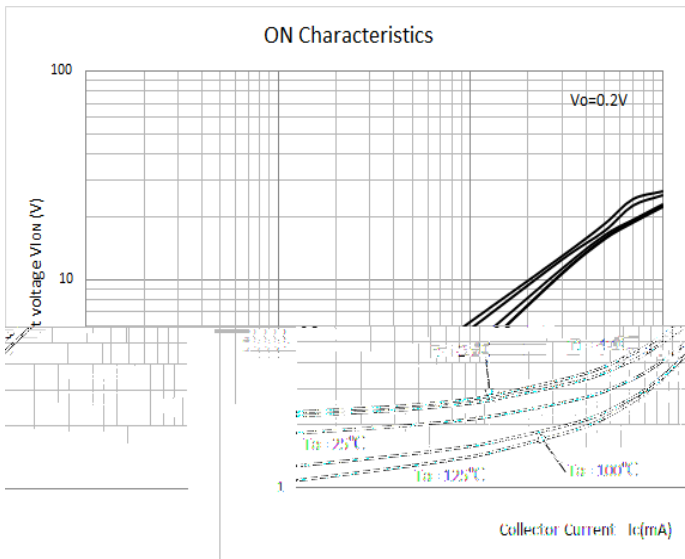
- 1 Device mounted on PCB, single-sided copper with standard footprint

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	UNIT WEIGHT(g)	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
DTC144WUA	F2	Approximate 0.005	3000	30000	120000	7

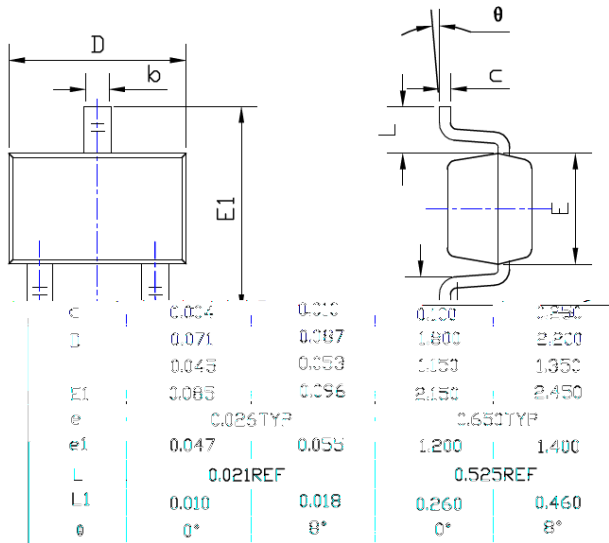


Characteristics (Typical)

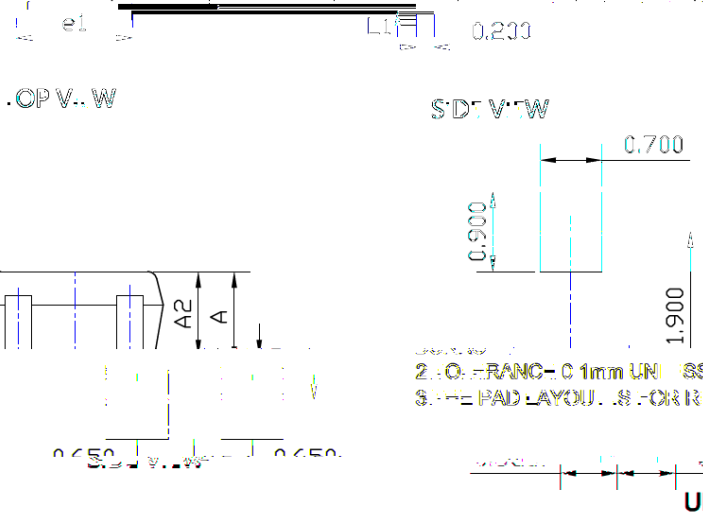




SOT-323 Package Outline Dimensions



SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.043	0.900	1.100
A1	0.000	0.004	0.000	0.100
A2	0.035	0.039	0.900	1.000
b	0.006	0.016	0.150	0.400



NOTE:
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE RIPPES

OR F R W S : S P C : H D .
G R I N G - P U R P O S E S O N L Y .

SIDE VIEW

2. O. T. T. R. A. N. C. = 0.1mm UNLESS
3. THE PAD LAYOUT IS FOR REF.

SUGGESTED SOLDER PAD L

UNIT: mm

LAYOUT

Note:

1. All dimensions are in millimeters (mm) unless otherwise specified.

[所有尺寸均以毫米为单位，除非另有说明]

2. General tolerances: ±0.10mm unless otherwise specified.

[通用公差为±0.10mm，除非另有说明]

3. Dimensions and tolerances per ASME Y14.5M-2018.

[尺寸和公差遵循 ASME Y14.5M-2018 标准]

4. Burr

maximum.

0.15mm]

0.100 mm per side.

ions of the

l flash,

mold mismatch.

以及胶体毛刺，

th respect to one another within a maximum

iting plane.

与0.1mm]

4. All dimensions should be exclusive of burrs and gate flash

Burrs and gate vestiges shall not exceed 0.15 mm in ma

[所有尺寸均不包括毛刺和浇口残留。毛刺与浇口残留的尺寸最大不得超过

5. Dimension b does not include dambar protrusion of max (

[尺寸b不包括单边最大0.100 MM的中筋凸出部分]

6. Dimensions D and E are the overall extreme outer dimens

mold compound. These dimensions exclude mold flash, leac

protrusions and burrs but include the maximum allowable r

[D和E是塑封体的外部极限尺寸，不包括包封溢料、内引线溢料、凸出部分

且包含了与封装溢料的尺寸部分]

7. Formed leads shall be planar wi

of 0.076 mm relative to the sec

[成型的管脚应为同一平面，共面性最大为

8. ★It is the key size.

[★ 标记为关键尺寸]

